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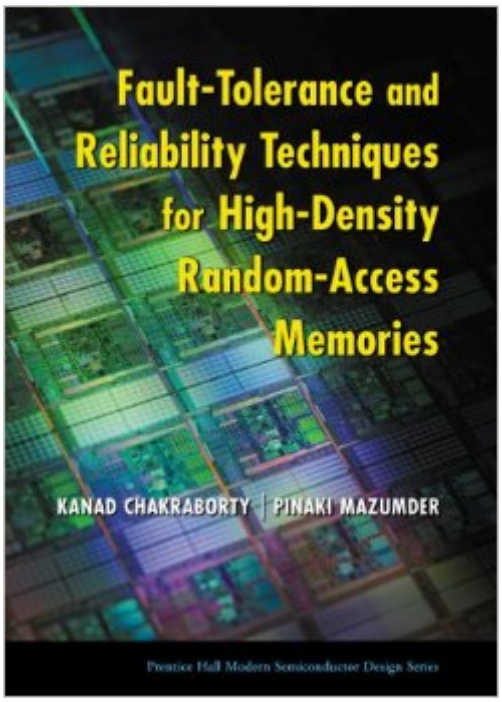

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Synopsis

Surveys the latest research and field-proven techniques for every form of memory fault tolerance, including manufacturing, online, and field-related fault tolerance. Authors focus on practical circuit and design solutions.

Book Information

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Archeologists today are in possession of clay tablets that still bear on their surface the symbols that were written on them over 6000 years ago. As a result of improvements in fabrication technology, today's integrated circuits can store many millions of times as much data in the same volume. Further improvements are expected - within 10 years it is expected that silicon chips with a billion transistors will be manufactured. The downside, of course, is that these circuits are extremely fragile. The stored data and the circuits themselves are prone to a host of destructive forces. For example, a single alpha particle does not pose a threat to the writing on a clay tablet, but can change a RAM-cell bit. The problem affects more than just the commodity memory industry, since a larger and larger portion of many kinds of chips consists of memory arrays.Over the years a vast amount of research has been dedicated to finding ways around this problem. This book, with a bibliography of 525 research papers, is a unique and comprehensive survey of the field. The mechanisms underlying hard and soft errors are described. The techniques for coping with these mechanisms include test and repair algorithms, built-in self-repair, reconfiguration, process and

circuit techniques, and error-detecting and correcting codes. The book can be useful for designers, manufacturing engineers, test engineers and researchers.

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